Exemption Request Form – Exemptions #15(a) & #15

Date of submission:

1. Name and contact details

1) Name and contact details of applicant

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On behalf of the Company/Business organisations/Business associations listed below participants in the **RoHS Umbrella Industry Project ("the Umbrella Project")**:

We will be inserting in this table endorsing Associations: (i) names, (ii) EU Transparency Register IDs (where applicable) and (iii) Logos.			

2. Reason for application:

Please indicate where relevant:

- ☐ Request for new exemption in:
- ☐ Request for amendment of existing exemption in:
- ☒ Request for extension of existing exemption in:
- ☐ Request for deletion of existing exemption in:
- ☐ Provision of information referring to an existing specific exemption in:
  - ☒ Annex III
  - ☐ Annex IV

No. of the exemption in RoHS Annex III or IV where applicable: #15(a) & #15

Proposed or existing wording: See proposed wording below

Proposed Wording for Categories 1 to 7, 8 including in vitro diagnostic medical devices, 9 including industrial monitoring and control instruments & 10:

Exemption		Scope **(for dates of applicability see "Duration where applicable" further below)**
15	Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages for bonding to cadmium zinc telluride (CZT)	Does not apply to applications covered by point 15(a) of this Annex. Applies to category 8, other than in vitro diagnostc medical devices
15(a)	Lead in solders to complete a viable electrical connection between the semiconductor die and carrier within integrated circuit flip chip packages where at least one of the following criteria applies: - a semiconductor technology node of 90 nm or larger; - a single die of 300 mm^2 or larger in any semiconductor technology node; - stacked die packages with die of 300 mm^2 or larger, or silicon interposers of 300 mm^2 or larger.	Does not apply to applications covered by point 15 of this Annex Applies to Categories 1 to 7, 8 including in vitro diagnostic medical devices, 9 including industrial monitoring and control instruments and 10

Duration where applicable:

We apply for renewal of these exemptions for the categories marked in section 4 further below for the respective maximum validity periods foreseen in the RoHS2 Directive, as amended. For these categories, the validity of these exemptions may be required beyond those timeframes. Although applications in this exemption renewal request may be relevant to other categories not marked in section 4 further below, this renewal request does not address those categories.

☐ Other: _____

3. Summary of the exemption request / revocation request

Solder bumps are minute solder spheres (typically ~80um in diameter) connecting a Silicon (or other semiconductor) die with a carrier in flip chip Application Specific Integrated Circuit (ASIC) packages. The bump solder joint is extremely sensitive: stress resulting from the large mismatch in the coefficient of thermal expansion (CTE) between the silicon (or other semiconductor) die and the carrier is concentrated at the small bump interface area and transferred by the bump to the fragile low-K dielectric layers inside the Semiconductor die. In addition, the hair- thin solder connection itself needs to withstand these high stresses.

Lead containing solder materials have been traditionally used to overcome the reliability challenges of Semiconductor flip chip joints. Lead- containing solder materials are softer and more ductile than lead- free solders. They have a better ability to absorb stresses resulting from CTE mismatch between semiconductor and carrier and transfer less stress to the low-K dielectric layers. In addition, they can better withstand stress and are less prone to solder cracking. Leaded solders can provide a lower melting temperature, thus require lower processing temperature creating less package stress. The use of leaded solders helps resolve failures such as cracks in low- K dielectric layers, solder cracks, silicon cracks, delamination and package warpage.Older flip chip product technologies, flip chip products with large die and large interposers for stacked die, are not able to meet long-term reliability requirements with lead-free solder bumps on the die. Older product technologies are defined as those having transistor gate lengths of 90nm and longer. Large die and large interposers are defined as being 300mm^2 (300 mm^2 for monolithic die and large interposers) or larger.

Flip chips are commonly used in long life, high reliability applications that remain in the field for over 20 years and require continuous availability as replacement parts. Legacy flip chip devices and many large die devices are older products that have declining volume year-on-year making it difficult to justify an all-layer and material redesign (this is usually not technically possible, as described in this renewal request). Removing these products from the market would create long supply gaps with minimal impact on the amount of lead in the EU market, but prevent the sale of many types of products in the EU.

Silicon technology nodes with transistor gate lengths longer than 250nm used aluminum interconnect in the wafer processing backend. Later on, industry had to migrate to copper interconnect due to device performance expectations and increased circuit densities. Devices on the 250nm to 90nm technology nodes converted to a common low dielectric constant film (low-k): fluorinated tetraethyl orthosilicate (F-TEOS). F-TEOS made copper interconnect possible. At the time, F-TEOS was a breakthrough in materials engineering and from an electrical perspective it reduced capacitance in the silicon wafer backend dielectric stack. Reducing the resistance of interconnect wiring and reducing the capacitance of the interlayer dielectric (ILD) allow for higher device clock speeds. Dielectric capacitance was significantly reduced with F-TEOS when compared to the dielectrics used earlier in the semiconductor industry. The porous nature of the film is what reduces the capacitance and F-TEOS offered improved electrical performance at the expense of film mechanical strength.

The low mechanical strength of F-TEOS makes it susceptible to dielectric fracturing beneath the under bump metallization (UBM) on the silicon chip (die) with lead-free wafer bumps, due to the increased stresses imposed. This does not occur with leaded C4 (controlled collapse chip connection) wafer bumps. Lead-free wafer bumps are significantly less ductile than those containing lead, and the observed failure mode mechanism is driven by coefficient of thermal expansion mismatch between the silicon die and the carrier which transfers the strain to the less ductile lead-free bump and the fragile F-TEOS dielectric. Fracturing of the dielectric with Pb-free wafer bumps is

commonly referred to as “ghost” or “white” bumps due to the way they appear by acoustic imaging. Not only can the failure mode reduce assembly yields, it can also adversely impact product reliability. The failure may not be caught when a unit goes through component assembly and final test. Compromised units that ship are at high risk of failing during the customer’s board level assembly process or in the field. The failure rates are unacceptably high. This failure mode does not occur with wafer bumps that contain lead because leaded bumps are able to absorb the stress associated with the coefficient of thermal expansion mismatch between the silicon chip and the substrate to which the solder attaches. Table 1 below compares the performance of the same product (with a die size of 98mm^2) – one with lead containing die solder to a version with lead-free die solder subjected to identical stresses. All units failed with lead-free die solder and there were not any failures with the leaded die solder.

Accelerated Stress	Process	Cycles	Temp Range (°C)	Rate of Temp Change °C/Min (Arbitrary Units)	Control Group Leaded C4 White Bumps (% Fail Units)	Pb-free C4 White Bumps (% Fail Units)
Level 0	After Die Attach	1	STD Pb-free C4 Reflow Temp	2.0 x "Y"	0%	0%
Level 1	MSL3 Reflow	3	STD Pb-free C4 Reflow Temp	3.5 x "Y"	0%	15%
Level 2	Air-to-Air Temperature Cycling (AATC)	*5	Covers Industrial and Commercial Requirements	"Y"	0%	100%

*Note: Commercial and Industrial AATC requires no failures at 400 cycles and 700 cycles, respectively.

Table 1: Product performance comparison

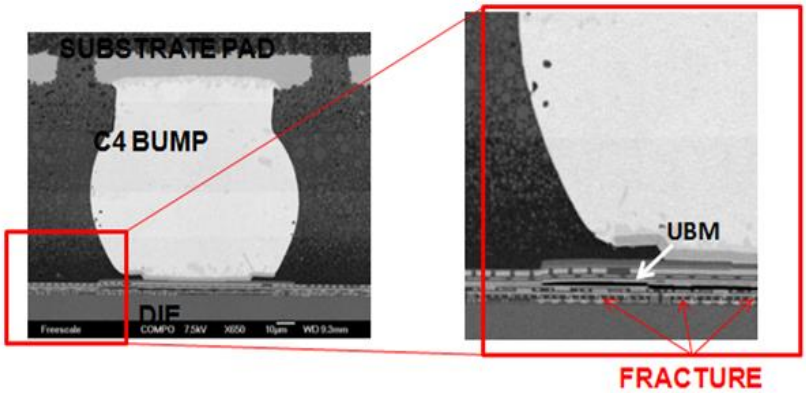

Figure 1: Dielectric fracturing using lead-free solder

Figure 1 is an example of dielectric fracturing using a lead-free solder bump.

Left Photo: Dielectric fracturing underneath a lead-free C4 wafer bump (“ghost” or “white” bump) after a chip (die) was assembled in a flip chip package. Thermal stress during the assembly process induces this failure mode. This does not occur with leaded C4 wafer bumps.

Right Photo: Magnified image of the dielectric fracture in the red box to the left. The arrows point to the delamination caused by package assembly with a lead-free wafer bump on a device with an F-TEOS backend wafer fab dielectric film stack.

Replacing the F-TEOS film with another ILD film is not an option. The entire backend wafer process integration would have to be re-engineered (e.g. dry etch; photolithography; film deposition; dielectric and copper polishes). Any change in the existing process architecture and materials would cause shifts in electrical characteristics that would force the device to have to be redesigned. There are many high reliability flip chip applications that continue to use these older silicon technologies

and they typically remain in the field for over 20 years. Examples of where flip chip packages are used include: microprocessors; routing switches; servers; broadband gateways; PBX; multiplex cards; printers; gaming applications; telecom; and a variety of wireless/RF applications.

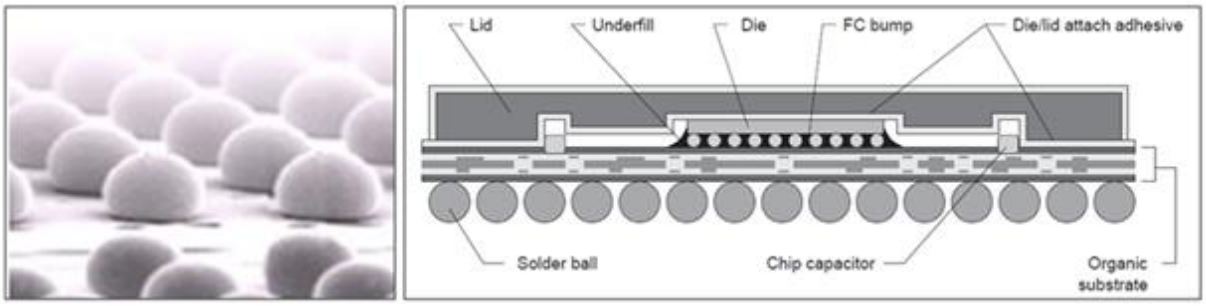

Figure 2: Flip chip solder bumps

Figure 2 provides a photo of solder bumps and the side view of a flip chip device.

Left Photo: Flip chip solder bumps on a silicon wafer (sphere diameters are typically 80 microns or less). Refer to Section 4.2 for a comparison of flip chip packaging to wire bond packaging. The solder spheres significantly reduce the length of the interconnect (wiring) between the silicon die and the substrate, required for achieving high clock rates.

Right Drawing: Illustration of a fully assembled flip chip package. The solder balls at the bottom are used to connect the package to the end users printed circuit board.

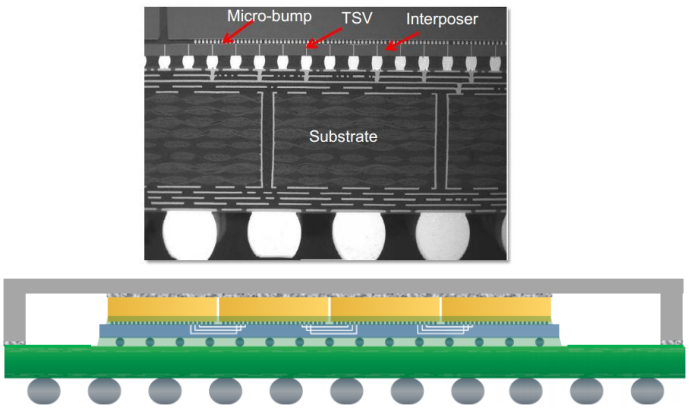

Figure 3: Stacked silicon 2.5D/3D package

Figure 3 images above: Cross-section of a Stacked Silicon Interconnect Technology (SSIT) or 2.5D/3D Stacked Die module with active die and passive interposer and finished package construction. Typical construction would be Cu Micro-bumps, 65nm Si technology and SnPb C4 bumps on the interposer. The finished package termination (BGA balls) would be Pb-free solder.

Over time, EEE consumers have expected improvements in both computing power and processing speed (i.e. higher clock rates). Transistor miniaturization and reductions in electrical resistance within semiconductor chips were required to accomplish this. Reduced electrical resistance was achieved in part by minimizing the interconnect wire length between the chip and the package. A repercussion of higher clock rates is increased power consumption by the chip which the packaged device must dissipate. Flip chip packaging was implemented to facilitate higher clock rates and heat

dissipation. For instance, microprocessors that clock between 1.4GHz and 3.8GHz must dissipate between 50 and 165 Watts of power over a very small area. Achieving device performance like this is not possible with wire bonding.

The most advanced silicon technology nodes, defined as those with transistor gate lengths of 65nm and smaller completely replaced F-TEOS. These replacement technologies are designed to address the stress levels associated with lead-free die solders, except when the die size is 300mm^2 or larger. Package size increases with die size and larger packages impart significantly more strain energy onto the die and solder bump. Consequently, lead-free die solder bumps are not compatible with large die sizes even in the most advanced silicon technologies. Large die with lead-free die solder bumps near the edges and corners will deflect much more thermal and mechanical stress during fatigue cycling which can cause brittle fracture in lead-free bump alloys.

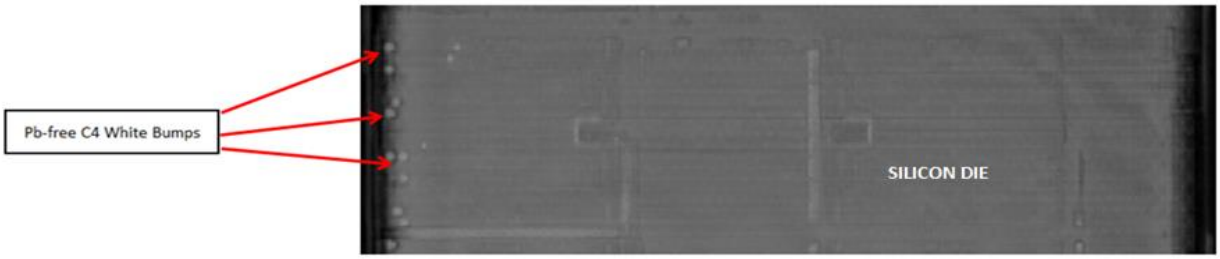

Figure 4: Pb-free C4 white bump image

Figure 4 image: White bumps at the edge of a die observed after Pb-free wafer bump die attach to a substrate. A white bump indicates a disconnect between the bump and the substrate, which causes device failure. This is a non-destructive imaging with a Sonoscan D9000 acoustic microscope.

Figure 5 illustrates innovations in materials and the materials process integration that are required in order to drive device performance and compatibility with lead-free solder bumps on die.

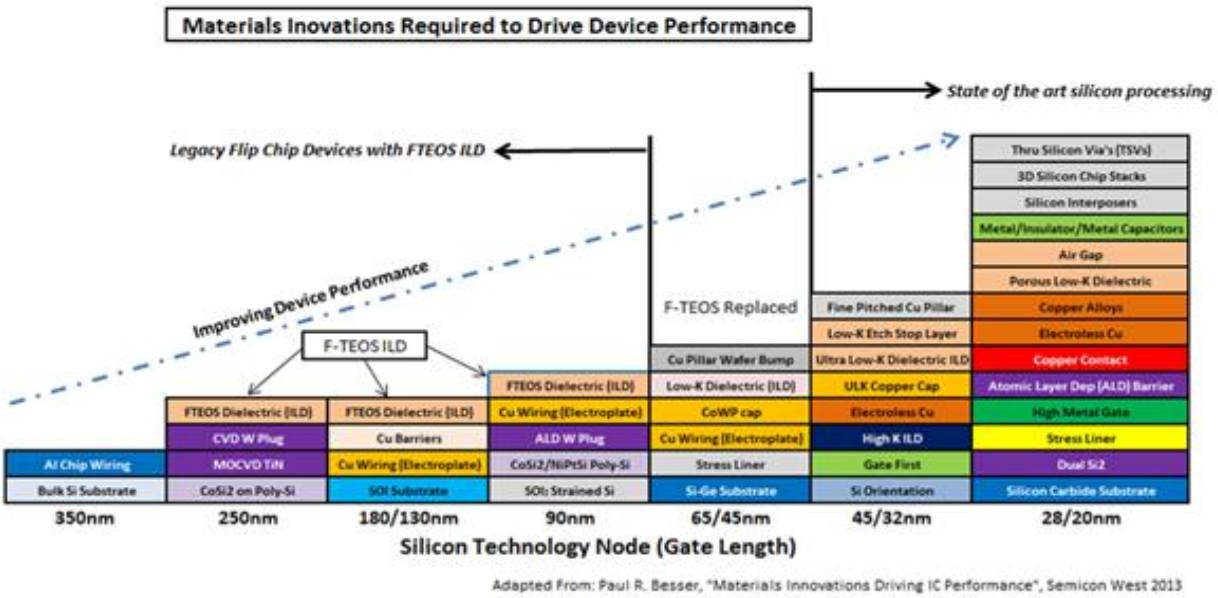

Figure 5: Innovations required for materials and process integration to enable lead-free bumping

This exemption renewal request describes one novel use of lead in flip chip bonds to cadmium zinc telluride (CZT) X-ray detectors used for medical imaging.

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4. Technical description of the exemption request / revocation request

(A) Description of the concerned application:

A. To which EEE is the exemption request/information relevant?
Name of applications or products:

Flip chip solders within active semiconductor components that require high speed and high reliability. These components are used in many types of EEE including the RoHS categories marked below.

i. List of relevant categories: (mark more than one where applicable)

☒ 1	☒ 7
☒ 2	☒ 8
☒ 3	☒ 9
☒ 4	☒ 10
☒ 5	☐ 11
☒ 6	

ii. Please specify if application is in use in other categories to which the exemption request does not refer: —

Applications in this exemption renewal request may be relevant to categories not marked above.

Applications in this exemption renewal request may be relevant to categories not marked above and below

iii. Please specify for equipment of category 8 and 9:

The requested exemption will be applied in
☒ monitoring and control instruments in industry
☒ in-vitro diagnostics
☒ other medical devices or other monitoring and control instruments than those in industry

2. Which of the six substances is in use in the application/product?
   (Indicate more than one where applicable)

   ☒ Pb ☐ Cd ☐ Hg ☐ Cr-VI ☐ PBB ☐ PBDE

3. Function of the substance:

   To complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages. A viable connection must support high speed electrical signal transfer, high heat dissipation, and/or be capable of high reliability and structural integrity during peak operating conditions.

4. Content of substance in homogeneous material (%weight):

   The flip chip Pb content is a sum of two parts. The flip chip semiconductor die bumps on the silicon chip vary from the general eutectic 37% Pb to > 85% Pb by weight. The flip chip bumps also require a Pb cladding on the substrate / interposer bonding pads or solder posts on the leadframe, generally using the 37% eutectic Pb, but could range much higher to meet production processing and reliability requirements such as thermal cycling demands. During the integrated package assembly process, the Pb will interact and form a single homogeneous substance. The exact Pb % weight in the solder after assembly will vary according to the bump size, pad size, and Pb % in each material type. The final Pb content will likely be less than 85% by weight.

Example of F/C Pb Materials	% Pb Content
Silicon Flip Chip Die Bump	37% - 97%
Solder Cladding on Substrate Pad* * May not be used for ceramic	37% - 75%
Combined Flip Chip Materials after Assembly	37% - 97%
Flip chip bumps to CZT	~34%

Table 2: Flip Chip examples of lead (Pb) content

5. Amount of substance entering the EU market annually through application for which the exemption is requested:

   It is currently estimated that approximately 85kg/year of lead is entering the EU due to the flip chip exemption.

   Table 3 below details the amount of lead estimated being shipped into the EU market. Estimates are based on WW shipments placed on the EU market. The 2008 through 2014 lead usage estimates from previous reports are included for reference

Total amount of lead (Pb) shipped to Europe (based on 25% of WW production)							
# devices (in millions)				Amount of lead (Kg)			
2008	2014	2018	2019	2008	2014	2018	2019
806	340	10.2	9.1	2315	896	112	85

Table 3: Estimated lead (Pb) containing devices and total lead shipped to EU

The 2018 and 2019 lead usage calculations were based on the following assumptions:

1. Wafer sales, both high Pb and Eutectic
   i. 200mm wafer size
   ii. Estimated average 350 units per wafer
   iii. Estimated average 1,25mg lead content per unit
2. 25% of WW shipments of flip chip are placed in the EU.
3. Volume estimates were obtained from TechSearch International

Overall lead usage for this exemption has continued to drop. From 2008 to 2014 it was reduced by 61%, from 2014 to 2018 it dropped another 87%. From 2018 to 2019 there was a 24% drop. As can be seen from this data, there is a trend of decreasing dependence on the use of leaded solder. The remaining devices using leaded flip chip attach are typically very large chips and/or long lived older IC technologies for which lead free designs could not be reliably produced.

The total lead amount in solder bumps is extremely small, having a minimal impact on the amount of lead in the EU market. For reference – approximately 216,500 large ASIC devices amounts to 10.0 kg of lead . This equates to approximately 20,000,000 small ASIC devices. Moreover, the lead containing bumps are located at an internal interface of the ASIC package and are encapsulated by a chemically stable polymer (underfill), significantly limiting impact on the environment.

Because of the long life-time of some devices and evolving IC manufacturing processes, devices manufactured in low volumes and used in specialist products that are made in small numbers, such as medical devices and test equipment, may require a "lifetime buy" when the older wafer fabrication processes are retired. In these cases, the manufacturers could be entirely dependent on existing inventory that has been manufactured with design rules that required leaded solders. If these devices are unable to be used in the manufacture of new products, these ICs would have to be disposed of and add to the electronic waste stream without contributing the value in which the products were intended before the product's useful end of life and the types of products that rely on them could not be sold in the EU. In addition, many existing products on which consumers and businesses are now dependent upon would become obsolete/waste due to unavailability of repair parts. Many of these devices with very large monolithic die were developed many years ago and are now sold in relatively small volumes. It would not be worthwhile for IC manufacturers to convert these devices to a Pb free bump package, even if this were technically possible, which as explained in section 6, is not technically possible. Due to the long qualification cycle for new of redesigned devices by IC manufacturers and also by end-users, it is likely that these components would become obsolete before qualification was completed.

6. Name of material/component:

   Pb solder within integrated circuit flip chip packages.

7. Environmental Assessment:

   LCA: ☐ Yes

   ☒ No

B. In which material and/or component is the RoHS-regulated substance used, for which you request the exemption or its revocation? What is the function of this material or component?

The lead (Pb) is a constituent of the solder used to form the viable connection between a semiconductor die and a carrier in flip chip packages.

C. What are the particular characteristics and functions of the RoHS-regulated substance that require its use in this material or component?

Lead containing solders are softer and more ductile than lead- free solders, thus better absorb stresses resulting from mismatch in the coefficient of thermal expansion between semiconductor die and carrier. Leaded solders transfer less stress to the low-K dielectric layers within the semiconductor die, reducing the risk for low- K layer cracking. They also better withstand the stress and are less prone to developing solder cracks. In addition, the lower melting temperature of eutectic tin-lead solders reduces the die attach reflow temperature, consequently reducing internal package stress during flip chip die attach.

Lower temperature melting solder minimizes internal package stresses that prevent package failures such as package material interface delamination, i.e., the glue under the chip delaminates from the package substrate. Due to its high reliability characteristics, especially in mission critical applications, this solution must remain unchanged during the life of customer's product line.

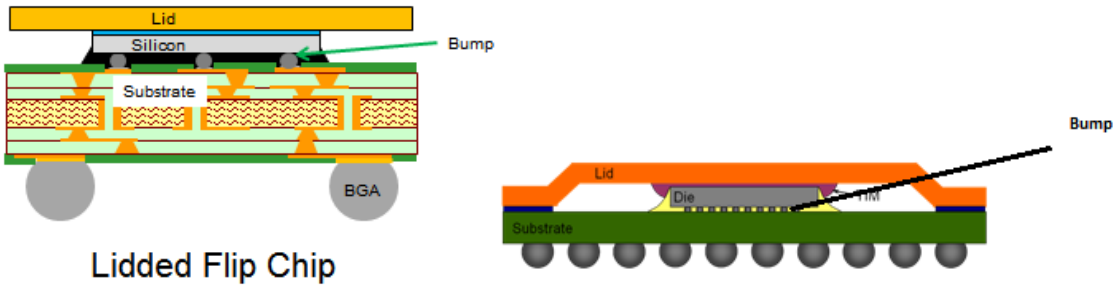

Figure 6: Examples of flip chip solder bumps used in products

Figure 6 demonstrates how lead (Pb) is used in flip chip products. In general,

- Flip chip bumps replace bonding wire and die attach material. The shorter interconnect is required for high speed devices
- Lead is required within internal solder joint to withstand higher reflow temperatures for subsequent processing

High lead content solders are employed in applications requiring the internal solder joint to withstand high temperatures during subsequent processing. The higher melting temperature of these solders enables the formation of a reliable joint, without deformation at high processing temperatures

Information below further describes renewal examples for each of the 3 definitions within Exemption 15(a). Please note, examples *are not* all inclusive.

Exemption 15(a) Definition 1: a semiconductor technology node of 90 nm or greater

a) Flip chip

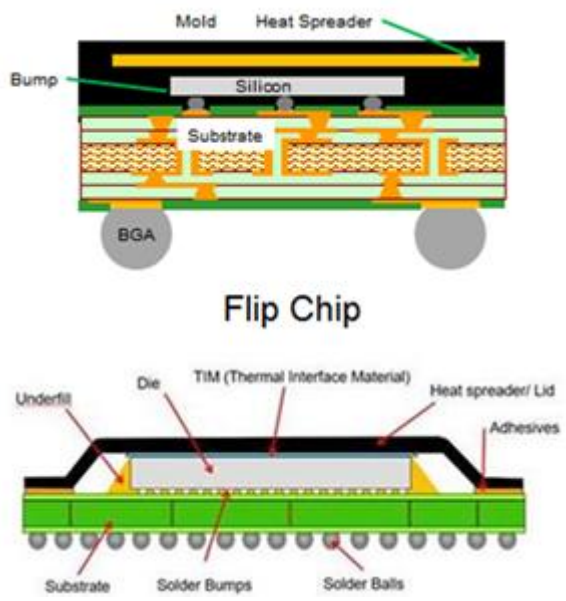

Figure 7: Examples of Flip chip packages

Figure 7 gives two examples of flip chip products that fall under the 90nm or greater technology node. As detailed in Section 1, these types of semiconductor devices use low – strength F-TEOS as low-K material. As a result, they are especially sensitive and experience low-K dielectric cracking at relatively low stress levels.

Exemption 15(a) Definition 2: a single die of 300 mm^2 or larger in any semiconductor technology node

The products falling under this category are the different types of Flip Chip (FC) Ball Grid Arrays (BGA).

Diagram example

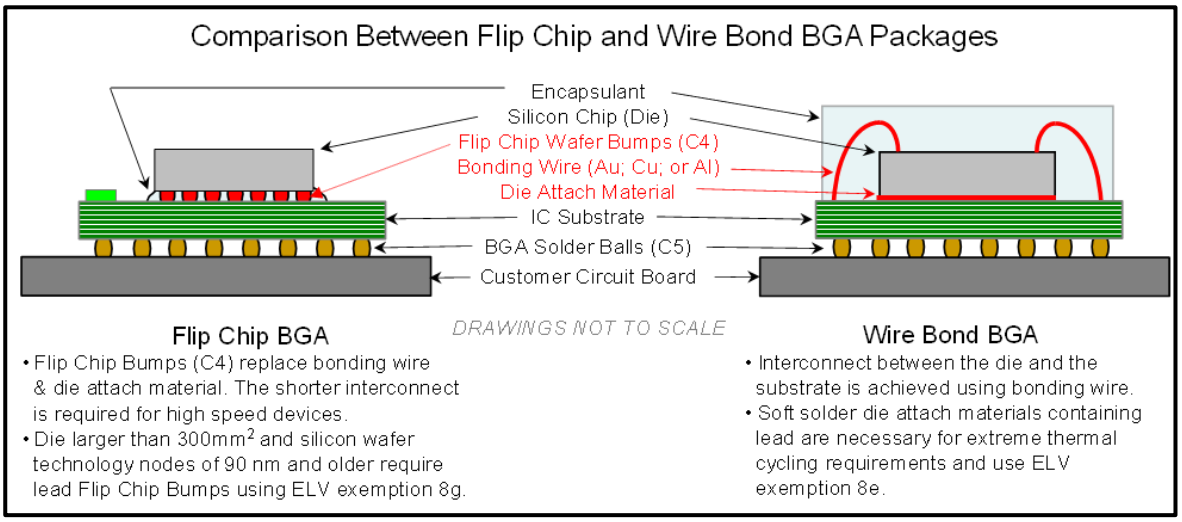

Figure 8: Examples of single die products of 300 mm^2 or larger

Figure 8 are examples of products falling under this category are the different types of Flip Chip (FC) Ball Grid Arrays (BGA). The flip chip bumps (also known as controlled collapse chip connection (C4) is a method to connect the semiconductor (die or silicon) to the substrate or carrier. These flip chip bump are manufactured with Pb alloy. The bump is used to replace the wire as the die is inverted when assembled in a flip chip package.

Package with Pb-free bumps on silicon up to 300 mm^2 die size has been qualified and are now in production. The shipment volume for these legacy devices with Pb bumps will decrease drastically over time in the next several years. New products introduced into the market in the last several years are assembled with Pb-free bumps even though the die size is greater than 300 mm^2.

Although the volume of these legacy Pb bump devices with large die (> than 300 mm^2) will be reduced in the next several years, there are many equipment manufacturers that are still using the legacy devices in small volume. Some of these devices are used in networking equipment and telecommunication products that have a long product life cycle. The semiconductor manufacturers have the obligation to continue to supply to these customers that have designed-in these devices with Pb bumps.

Even if a Pb free solution may be available, which for many products is not the case, qualifying a legacy device with a Pb free bumps is economically not feasible for these equipment manufacturers due to the high mix and low volume type of product offering.

Exemption 15(a) Definition 3: stacked die packages with die of 300 mm^2 or larger, or silicon interposers of 300 mm^2 or larger

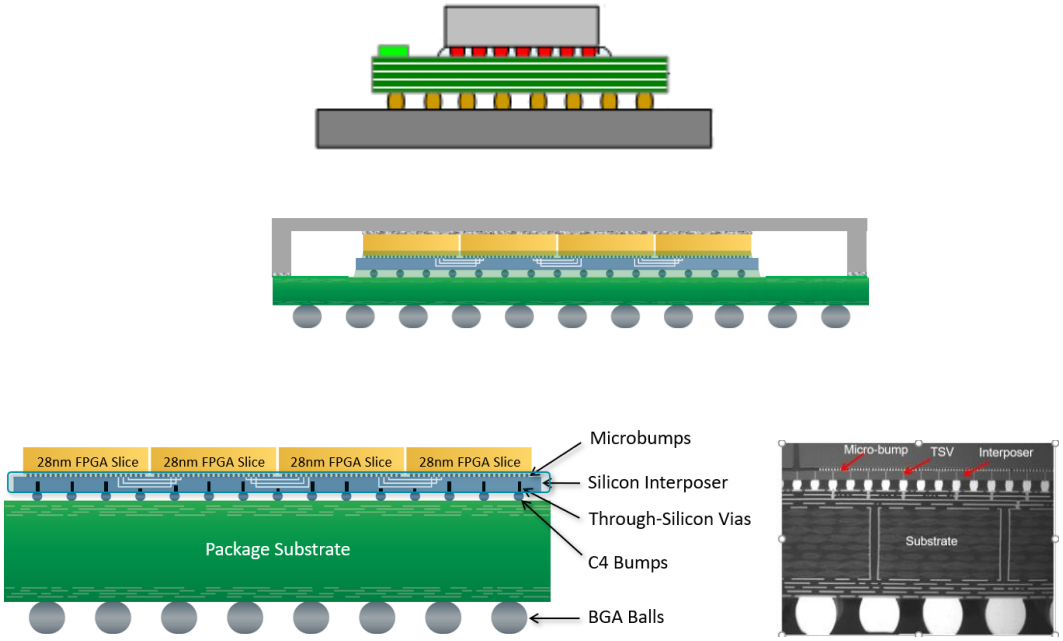

Figure 9: Examples of stacked die packages with Large Interposers

The images within Figure 9 represent the schematic side view of a stacked silicon interposer package containing four active silicon dies connected to each other through a passive interposer with through silicon via (TSV) using micro-bumps. In this type of package, any number of active dies can be assembled on the interposer and can then be connected to an organic package with C4 bumps. A capillary underfill is used to fill the gap between the micro-bumps and interposer, which helps in reducing the stress in micro-bumps. C4 bumps are created on the interposer backside, which are connected to a package substrate. A second layer of C4 bump capillary underfill is used to fill the gap between the interposer, C4 bumps and the organic package.

The warpage of such stack die on interposer packages are inherently higher due to presence of multiple underfill material and copper TSV structures. Transition to lead free solder would require alternate higher Tg underfill which further make warpage worse. Higher warpage adds significant stress to the package causing underfill delamination leading to bump cracks and silicon LoW-K cracking. In addition to this, the use of lead free solders and associated underfill materials also increases the coplanarity of the device. High coplanarity causes significant challeneges for end user during the board attach process causes non wet and HIP joints. Hence lead-free solders cannot be used with stacked die packaged with interposers of 300 mm² size and larger.

Renewal of exemption 15 for Category 8

Exemption 15(a) is acceptable for Category 8 components except for the one use given below where Exemption 15 is required. Exemption 15 renewal is required for one category 8 use of specific flip chip bonding to CZT (cadmium zinc telluride) for ionising radiation detectors

CZT is a specific type of integrated circuit (IC) flip chip package that consists of a CMOS (complementary metal–oxide–semiconductor) die, typically CZT or cadmium telluride that is bonded on the underside CMOS circuit of the crystal using lead alloy “bump bonds” to attach it to the carrier circuit, reference Figure 10 below. These detectors are used in Computed Tomography (CT) machines that are used for 3D X-ray imaging of patients. CZT X-ray detectors give superior image quality with lower radiation doses compared to other types of detector. The CZT die is heat and stress sensitive so that the solder used must have a melting point as low as possible and be very ductile. Each die has an area of about 200mm^2 and the CMOS circuitry will use <90nm technology node. To generate high definition images, multiple dies are used to obtain a large area detector for very good image resolution and quality. The image below[1] shows a prototype ASIC (Application-Specific Integrated Circuit) carrier circuit, onto which the CZT crystal will be solder bump-bonded.

[1] As published in Nuclear Instruments and Methods in Physics Research A862 (2017) 18–24)

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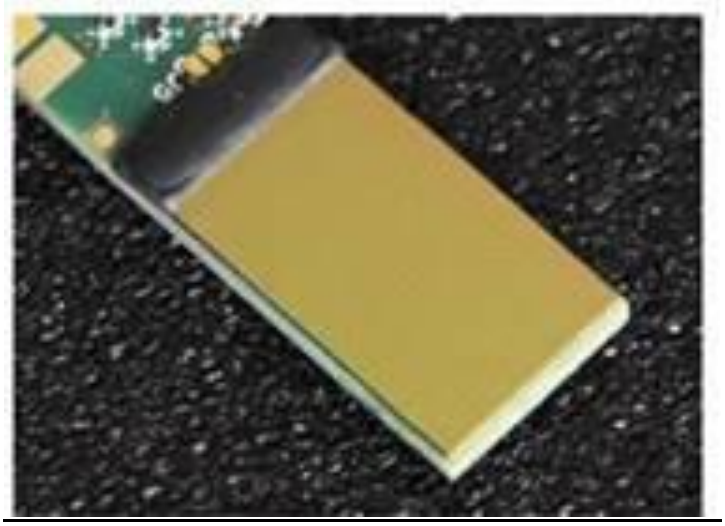

Figure 10: Circuit board with carrier circuit onto which the CZT semiconductor crystal is flip-chip bonded

Additional requirements for flip chip bonding between CZT ionising radiation detectors to carrier circuits:

- Melting point of <120°C
- Must be very ductile
- Constituents of the alloy must not diffuse into direct conversion sensor as they can destroy its function

Exemption 15(a) is very widely used in medical devices. Medical device manufacturers use the same components as all other sectors of the electronics industry but can be seriously affected by early obsolescence of components (if drop-in replacements are not available) , as redesign of medical devices involves retesting, sometimes clinical trials and they need to gain approval from Notified Bodies before redesigned products can be sold. This can mean that some products are no longer sold in the EU which limits the choice of hospitals and this can negatively affect healthcare.

5. Information on Possible preparation for reuse or recycling of waste from EEE and on provisions for appropriate treatment of waste

1) Please indicate if a closed loop system exist for EEE waste of application exists and provide information of its characteristics (method of collection to ensure closed loop, method of treatment, etc.)

No closed loop system exists for waste collection on flip chip integrated circuit packages, however end of life EEE follow EEE recycling scheme. EEE are separately collected and sent for recycling to specialized centers. All centers are able to separate Pb with other metals into a fraction that can be used again.

These components are recycled as part of the EEE into which they are incorporated. However, it should be considered the event of disposal the solder in a flip chip device inherently presents a much lower risk to the environment than many other uses of lead alloys. Flip chip devices are typically “under filled” with a chemically stable epoxy encapsulant that seals in the solder. The volume of solder used in these devices is also very small. The largest of the monolithic die that is in production with Pb-bump solution is about 750 mm^2. For this die, the amount of Pb in the package is estimated to be about 45 mg. The amount of lead in smaller flip chip devices are in the 0.5 mg range. The annual number of flip chips sold in Europe are 499 million (2018 estimates from Table 3).

2) Please indicate where relevant:

☐ Article is collected and sent without dismantling for recycling

☐ Article is collected and completely refurbished for reuse

☐ Article is collected and dismantled:

- ☐ The following parts are refurbished for use as spare parts: _____
- ☐ The following parts are subsequently recycled: _____

☐ Article cannot be recycled and is therefore:

- ☐ Sent for energy return
- ☐ Landfilled

3) Please provide information concerning the amount (weight) of RoHS substance present in EEE waste accumulates per annum:

☐ In articles which are refurbished _____

☐ In articles which are recycled _____

☐ In articles which are sent for energy return _____

☐ In articles which are landfilled _____

6. Analysis of possible alternative substances

(A) Please provide information if possible alternative applications or alternatives for use of RoHS substances in application exist. Please elaborate analysis on a life-cycle basis, including where available information about independent research, peer-review studies development activities undertaken

As is the case with most electrical equipment manufacturers, for legacy packages requiring these exemptions, there is no direct Pb-free solution available. The lead (Pb) used in these packages resolved failures such as delamination, die crack and bump cracking being seen by any other solution when designed 10 or more years ago.

Pb-free efforts were focused on Package redesigns that have increased the overall component's diameter, thickness and/or ultimately mass compared to the previous Pb containing packages. These new packages also have different functions. Since the newer package solutions cannot maintain the form, fit and function of the legacy package technology, they are not drop in replacements.

Flip chips with 90nm (or older) technology node have relatively lower bump density (number of bumps per die area) compared to those of newer technology nodes. The newer technology nodes would eventually have more logic elements, which require more IO pins for transmitting the signals (eventually more bumps in a dense area), as compared to older technology node (less logic elements equates to lower bump density per die area).

The fewer number of bumps per die area has resulted in higher stress per bump. This mitigation would require potential changes in new materials and process optimization like aluminum thickness, passivation layer, polyimide layer, bump layout, underfill material, substrate composition in order to prevent failures due to the stress on the bumps.

Investigations for lead-free solutions for the flip chip application within the > 90nm process are moving forward. The changes requires many material changes to enable the move to a Pb-free solution:

- Material changes include: flux, underfills, and mold compound materials compatible with Pb free conditions
- Improved assembly process conditions: flux clean and plasma prior to underfill step that address Pb free conversion challenges
- Transition of substrate materials to lower TCE/ higher modulus materials
- Higher Pb free temperature in the assembly process requires assembly performance improvements: optimized reflow to address non-wet solder and bump voiding, improved underfill adhesion, and reduction of mold resin bleed are a part of the on-going manufacturing learning cycles.

Development costs for new flip chip devices are likely in excess of $50M[2]. In the case of high volume consumer devices, these costs can be recovered in a relatively short period of time due to very high product volume. Because of competitive pressure, these devices will often have a life cycle of less than 18 months on the market. For lower volume devices that do not require the increased performance of the latest IC technology, the industry relies on a long product life to offset the high development and tooling cost. In the case of server and telecommunication business, many of the integrated circuits will be used for 7-10 years with only minor design changes. To maintain Form, Fit and Function minor changes cannot be ones that

1. Modify the devices height, width or length
2. Change how the connections from the device to the printed circuit board fit together.
3. Significant material changes that can affect the functionality of the device in its current package design. Going from Lead to a non-Lead solution is a major material change.

If these devices were to be continually migrated to the latest IC fabrication process, the cost of designing new ICs and qualifying them in the systems would be prohibitive for many products.

The industry has demonstrated a strong commitment to developing new lead free flip chip devices as new technologies become available. Where it has not been feasible to move old designs into new IC technologies, the remaining devices present minimal risk to the environment. The remaining devices manufactured in leaded flip chip attach are expected to decline steadily over time as those products are replaced with newer technology.

Therefore renewal is required for these exemptions since the substitution of lead in FCP in scope of exemption 15a is not possible due to the poor reliability of substitutes which is described in section 6 (B).

Assessment of substitute bonding to CZT die for X-ray imaging applications

The cadmium zinc telluride (CZT) die may be damaged by temperatures of >120°C as the properties and performance would be adversely affected and so solders such as eutectic tin/lead solder (melting temperatures 183°C) and the commonly used lead-free solders, such as tin-silver-copper (melting temperatures of about 218°C) cannot be used as flip chip bonds to the underside of the crystal as melting these solders require significantly higher temperature. The solder alloys that have been found to be suitable are bismuth-tin-lead (ca. 34% lead) which have a melting point of 96 - 105°C. The only lead-free solder alloys that have low melting points and are sufficiently ductile contain indium, such as 54%Bi 29.7%In 16.3%Sn (m.pt. 81°C eutectic), which is too low as there is

[2] Citing International Business Strategies Inc. (IBS), a research firm, Cadence's Beckley said at the 32/28nm nodes, a fab runs $3 billion, process R&D is $1.2 billion, IC design costs ranges from $50 million to $90 million, and mask costs are from $2 million to $3 million"

a risk of melting due to internally generated heat and when the equipment is used in hot climates. The other potential alloy InSn alloy has a m.pt. of 125°C, which is above the upper 120°C upper limit. However, it is also known that indium metal electrodes may diffuse into the CZT substrate and would destroy the “blocking contacts”. Blocking contacts are used on semiconductors to prevent atoms (e.g. from bonding materials) from diffusing into the semiconductor and destroying their function[3]. Therefore, alloys containing indium cannot be used as they could cause poor reliability and shorten lifetimes and alloys containing lead can be used as only these have all of the essential requirements.

Bonding of CZT using anisotropic conducting adhesives is described in research publications and initially gives suitable electrical connections. However, with CT, the CZT detector assembly is exposed to very intense ionising radiation (from the X-rays used for imaging) which will destroy the adhesive and this would cause the electrical bonds to be lost as the adhesive decomposes.

(B) Please provide information and data to establish reliability of possible substitutes of application and of RoHS materials in application

The use of lead free solder bumps in flip chip interconnects continues to be a challenge. Reliability concerns are well documented with the use of lead free solders because they are less ductile than lead solders (several examples of failures are described above). This causes the lead free solders to crack under stress and increases the likelihood for failures during the product life cycle. Preventing lead free solder cracks requires additional engineering to improve the thermal and mechanical fatigue life of the solder joints. The primary solution is a load-transfer from the solder to an underfill encapsulant. The residual stress from the underfill can cause other material failures which most commonly include dielectric crack, delamination or die crack. Each component must be redesigned and tested several times to obtain the correct formulation needed to protect each layer and the solder joints.

Standard characterization requirements have shown an increase in the positive performance criteria:

- Initial extended temperature cycling to 2,000 cycles have been fail free at -55°C to 125°C conditions
- Standard HTS and uHAST testing has shown positive results
- Board level reliability (BLR) is also being performed with positive results
- Verification is being made with tools such as X-ray and C-SAM analysis at the specified qualification check points

[3] One publication states that indium dopant in CZT increased electrical resistivity threefold which would be expected to be detrimental to CZT as an X-ray detector. https://www.researchgate.net/publication/223200104_Effects_of_In_doping_on_the_properties_of_CdZnTe_single_crystals

Solutions for large die sizes (>300 mm^2) are not available due to the increased internal stresses that require more precise engineering to prevent the same failures from occurring. When using lead free solder with large die, industry has experienced similar failures as previously mentioned, and has experienced less common failures as discussed below.

Large die with lead free bumps requires a high glass transition temperature (Tg > 120°C) underfill (UF) to prevent solder bumps from cracking during stress tests. Figure 11 shows a typical high Tg UF with a large modulus (>10 GPa) at low temperature (<0°C). The DMA stress-strain curve shows that the storage modulus increases as the temperature decrease. The high Tg UF becomes very rigid at lower temperatures and the loss of flexibility places strain on the substrate solder mask.

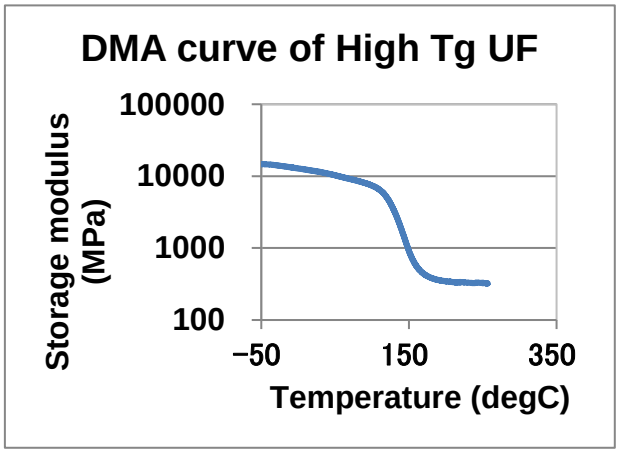

Figure 11: Typical DMA curve of High Tg underfill

The solder mask layer is an organic polymer used for its insulating properties to prevent solder migration. The solder mask ensures a proper connection is made between the solder bump and substrate pad.

Figure 12 and Figure 13 show that during reliability temperature cycling from -40°C to -50°C for large die the solder mask will crack due to the high stress imposed by the high Tg UF.

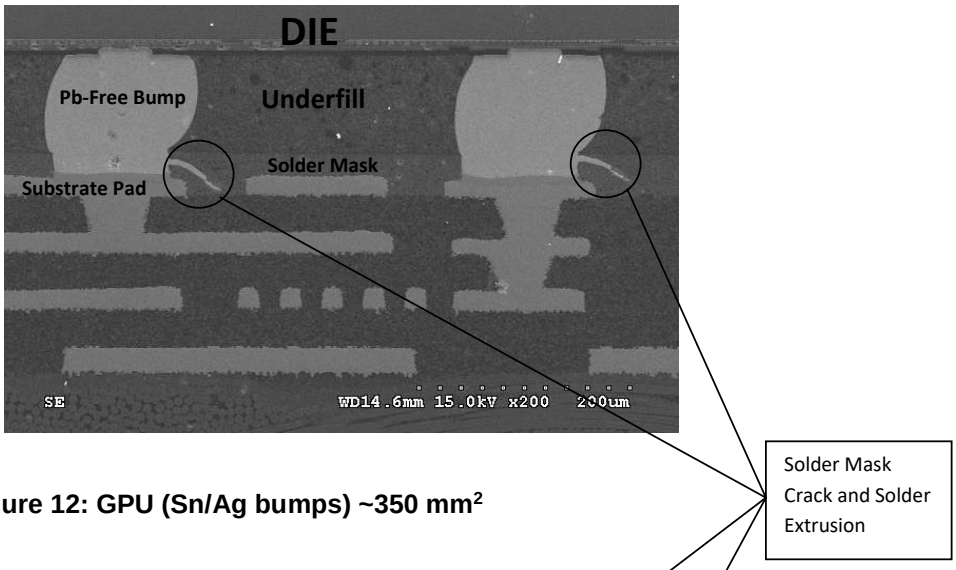

Figure 12: GPU (Sn/Ag bumps) ~350 mm²

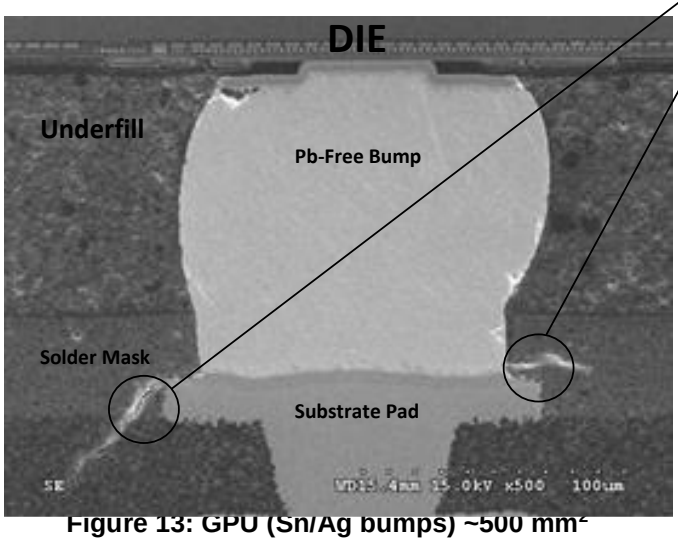

Figure 13: GPU (Sn/Ag bumps) ~500 mm²

The crack allows for solder to extrude through the solder mask. The solder extrusion significantly decreases the package reliability due to open-short failures.

The failures shown above demonstrate that the additional strain from large die increased the failure rate for the solder mask. Ultimately, this adds another variable to the equation in developing a solution to use lead free solder or any substitute interconnection technology for large die. Our research and development is still on-going and more time is needed to find a reliable lead free solution.

References:

https://www.techdesignforums.com/practice/technique/five-key-challenges-20nm-custom-design/

Challenges Associated with Large Stacked Die Flip Chip Package Assembly:

Figure 14 shows the schematic side view of a stacked silicon flip chip package. In this package, four active silicon dies are connected to each other through a passive interposer with through silicon via (TSV) using micro-bumps. In this type of package, any number of active dies can be assembled on the interposer and can then be connected to an organic package with C4 bumps. A capillary underfill is used to fill the gap between the micro-bumps and interposer, which helps in reducing the stress in micro-bumps. C4 bumps are created on the interposer backside, which are connected to a package substrate as shown in Figure 4. A second layer of C4 bump capillary underfill is used to fill the gap between the interposer, C4 bumps and the organic package.

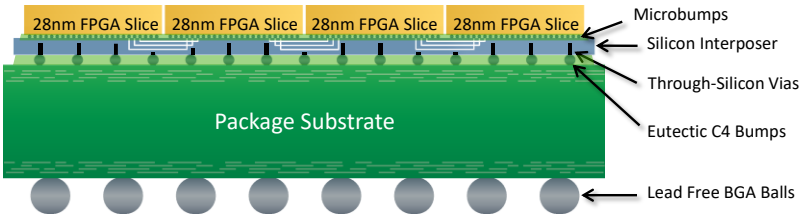

Figure: 14 Schematic Side View of Stacked Die Package or Stacked Silicon Interconnect Package without Lid

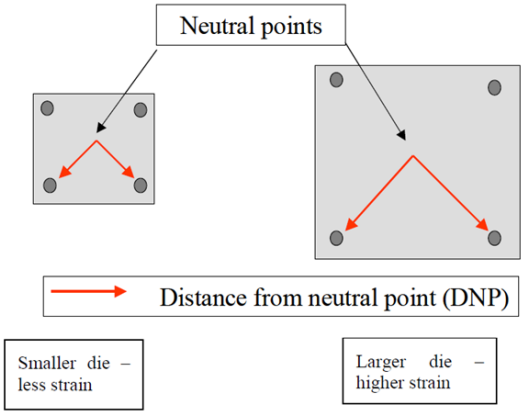

Figure 15 - Dependence of Die Size on Level of Strain (Shown by Arrows) On Corner Bumps

Size of strain on bumps is dependent on the die size and the laminate material. Most laminates have similar thermal coefficient of expansion (TCE) which is ~15ppm/°C whereas silicon has TCE of ~2.5ppm/°C. The size of the strain on bumps located at opposite corners is proportional to die size. This is referred to as the distance from the neutral point (DNP), where there is no stress at the centre of the die (DNP).

Strain is imposed by several mechanisms including device fabrication. It is particularly severe however when the component's temperature changes as a result of differential thermal expansion. When temperature increases, the laminate expands more than the silicon and this applies a strain to the solder bump and to the materials to which these are attached.

This strain can cause damage to:

- The dielectric material that is used as insulating layers on the silicon die surface, especially if low-k dielectric materials are used.
- The solder bonds to silicon die and to carrier circuit as a result of thermal fatigue
- The silicon itself which may crack

As the silicon die and carrier PCB are rigidly held by the solder bumps, the effect of differential thermal expansion is to apply an outward strain on the solder bump bonds as shown by the arrows in Figure 15. The applied force is partly relieved by distortion of the silicon and package, which can "bow" outwards similarly to a "bimetallic strip" that bends when heated as a result of the different TCE values of the two metals. Therefore, as the expansion of the polymer laminate is constrained by the low TCE silicon this results in warping of these two materials. Warping causes tension on joints which can cause cracking. Underfill materials are injected between the die and carrier package to reduce strain imposed on solder bumps by spreading out the forces induced by differential thermal expansion. Underfills are designed to put solder bumps into compressive strain which prevents fatigue failure but they also increase the overall stress to the package because they have larger TCE values than the carrier material and this causes warping.

Eutectic tin/lead[4] is a soft ductile alloy that forms strong bonds. High ductility is important as the solder deforms when a strain is imposed as a result of temperature due to the differential thermal expansion of silicon and carrier. Deformation of the eutectic tin/lead solder bumps when strain is imposed reduces the maximum level of strain on the solder joint and to the dielectric layers that form the circuitry on the silicon die. Calculations show that the maximum strain on joints imposed during thermal cycles when tin/lead solder is used is far lower than when the harder lead-free solders are used.

Lead free solders usually require underfills with higher Tg and higher modulus than eutectic solder. The main side effect of the higher Tg and modulus is that it imparts higher stress in the package which results in higher overall package warpage. The room temperature coplanarity of a lead free stacked die package is almost two times higher than that of stacked die package with eutectic C4 bumps.

The distortion from warping causes cracking and delamination of low k dielectrics and detrimentally affects the planarity of the level 2 solder balls. If the level 2 balls do not lie in a flat plane, some (usually those in the middle) will not make contact with the PCB causing open circuits. The

[4] Tin/lead and lead-free solders comparison: Jean-Paul Clech, "Acceleration Factors and Thermal Cycling Test Efficiency for Lead-Free Sn-Ag-Cu Assemblies", SMTA International Conference, 2005

coplanarity of the lead free stacked die package is significantly higher than 8 mils. Research has shown that if the co-planarity of solder balls can be kept within 8 mil (0.2 mm) good bonding to the PCB is possible whereas worse co-planarity values indicate a high risk of open circuits. This value has been included in a standard published by JEDEC (Design Standard 95-1).

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7. Proposed actions to develop possible substitutes

(A) Please provide information if actions have been taken to develop further possible alternatives for the application or alternatives for RoHS substances in the application.

As described in Section 6, substitutes for leaded solders are being developed by the industry for new designs, these solutions require implementation of multiple changes in package materials and die design. Among other - removal of solder bumps from high stress locations, use of underfill materials with higher glass transition temperature (Tg) which are able to off-load the stress from the solder joint, and use of lower TCE carrier dielectrics.

Implementation of the above mentioned solutions to legecy products is not possible, or will require extensive re-design and re-qualification. The cost of re-designing and re-qualifying these products is extremely high, reaching $1Million per product at component level only. Such high cost can not be justified for legacy products manufactured in small quantities and over the prime of their life-cycle. Neither do viable alternatives exist to replace legacy ASICs, as no drop-in pin-comatible replacements, meeting same form fit and function exists. The cost of re-designing and re-qualifying existing systems to operate with alternative solutions is even higher than the cost at cmponent level. Thus, for legacy products not originally designed to meet long-term reliability requirements with lead-free solders, no alternatives exist.

Conversions where possible, require a major change of all materials currently being used. The industry is continuing to research Pb-free solutions using new materials and process techniques. These solutions

1. cannot change product footprint
2. must maintain compatibility with package designs
3. must meet or exceed current form / fit / function requirements.

The Cu, SnAg and SAC are more rigid than the Pb flip chip solder, introducing more stress on the products. For older technologies, large die sizes, and large interposers for flip chip stacked die this additional stress ultimately results in an unacceptably high product failure rate

The electronics industry has demonstrated a strong commitment to developing new lead free flip chip devices as new technologies with adequate reliability become available. The remaining devices manufactured in leaded flip chip attach have proven to be much more difficult or impossible to substitute. Sales of older designs of components are expected to continue declining as those products are replaced with newer technology, assuming that this research is successful.

(B) Please elaborate what stages are necessary for establishment of possible substitute and respective timeframe needed for completion of such stages.

Fabricators and end users of flip chip ICs require time to qualify new processes and materials, redesign equipment and carry out performance and reliability testing. For some types of equipment such as medical devices, approvals are needed globally before redesigned or new products can be sold. Once successful component qualifications have been completed, a transition period will also be required for users of these products to re-qualify their products with the lead-free version, which can take a minimal of 5 years for typical applications and much longer for medical appilcations if redesign is neccessary.

Flip chip bonding of CZT ionising radiation detectors

As stated in previous sections, the only alternative solders with sufficiently low melting and having good ductility contain indium, which is an unsuitable solution. Other bonding methods

could be investigated, such as anisotropic conducting adhesives (as described in section 6), but are less likely to be reliable due to the intense vibration and stresses that occur in CT (computed tomography imaging) as well as due to the decomposition of the polymers in these adhesives that will occur from exposure to X-radiation. Any R&D into alternatives will take at least 5 years. In addition, these options will have to be tested in CT, clinical trials carried out and global approvals obtained, taking in total at least 10 years from now. Considering:

- the small amount of lead used and the non-existing impact for environment and human health
- the high costs for a 5 year R&D program would divert resources from innovation
- the fact that substitution would not improve the performances of the detector and that resources could be better spent researching the next generation detector technology

There is a need for manufacturers‘ continued Pb flip chip use until the end-of-life of their equipment. In addition, the spares required must be the same Pb flip chip Even if a technical solution exists to convert all the Pb flip chip to Pb free flip chip, the equipment manufacturers still have to qualify the newly redesigned Pb free flip chip. The qualification cycle can be very long and by the time the Pb free flip chip are qualified, the Pb parts would be approaching the end-of-life.

8. Justification according to Article 5(1)(a):

(A) Links to REACH: (substance + substitute)

1) Do any of the following provisions apply to the application described under (A) and (C)?

- ☐ Authorisation
- ☐ SVHC
- ☐ Candidate list
- ☐ Proposal inclusion Annex XIV
- ☐ Annex XIV
- ☐ Restriction
- ☐ Annex XVII
- ☐ Registry of intentions
- ☐ Registration

2) Provide REACH-relevant information received through the supply chain.

Name of document:

Based on the current status of Annexes XIV and XVII of the REACH Regulation, the requested exemptions would not weaken the environmental and health protection afforded

by the REACH Regulation. The requested exemptions are therefore justified as other criteria of Art. 5(1)(a) apply

(B) Elimination/substitution:

1) Can the substance named under 4.(A)1 be eliminated?
   - ☐ Yes. Consequences? _____
   - ☒ No. Justification see 6 and 7
2) Can the substance named under 4.(A)1 be substituted?
   - ☐ Yes.
     - ☐ Design changes
     - ☐ Other materials
     - ☐ Other substance
   - ☒ No.

     Justification see 6 and 7
3) Give details on the reliability of substitutes (technical data + information)

   See reliability data under question 3.
4) Describe environmental assessment of substance from 4.(A)1 and possible substitutes with regard to
   i. Environmental impacts : _____
   ii. Health impacts : _____
   iii. Consumer safety impacts : _____

   1) Do impacts of substitution outweigh benefits thereof?

Please provide third-party verified assessment on this: _____

(C) Availability of substitutes:

1) Describe supply sources for substitutes: No substitutes exist for the revised narrow flip chip scope as described in Section 2.
2) Have you encountered problems with the availability? Describe: _____
3) Do you consider the price of the substitute to be a problem for the availability?
   a. ☐ Yes ☒ No
4) What conditions need to be fulfilled to ensure the availability? _____

(D) Socio-economic impact of substitution:

1) What kind of economic effects do you consider related to substitution?

☒ Increase in direct production costs

☒ Increase in fixed costs

☐ Increase in overhead

☒ Possible social impacts within the EU

There could be serious implications in the EU if this exemption is not renewed as many products rely on this exemption. EU industry would become less competitive if equipment is available outside of the EU but not in the EU. This is particularly important for specialist monitoring and control equipment where redesign, testing and gaining approvals can take a minimum of five years and if EU sales are small (many examples of industrial category 9 products are sold at <100 per year and some are <5 per year), non-EU manufacturers may decide not to continue to supply the EU. EU citizens' health could also be affected if these types of medical devices could not be sold in the EU.

The example below explains why not renewing exemption 15a would harm EU citizens.

To eliminate this exemption for all devices prematurely would have significant socioeconomic risks associated with early retirement of critical technologies, placing EU countries at a competitive disadvantage and potentially harmful to EU hospital patients if new medical devices are not available.

The flip chip packages used in medical devices are usually unique and cannot be replaced by different lead-free flip chip packages. For example, flip chip packages are used in intravascular ultrasound (IVUS) imaging. Eliminating the lead bumps would only be possible by a complete redesign of all of the IVUS equipment. When a medical device is redesigned or significantly changed in any way, the modified product cannot be sold in the EU until it has been approved by a Notified body. Notified body approval is granted only if the manufacturer has proven that:

- its performance is as good as the previous version
- It is no less reliable
- Patient's health will not be harmed

To redesign a product, it requires, extensive testing, reliability trials and sometimes clinical trials. This is impractical for mature products because:

- Field data shows that the existing product is reliable, but there will be uncertainty over any new design
- It is likely that the current product model will be due for replacement by a new

more sophisticated superior performing model by the time that a redesign is complete and approval granted. Therefore, it is more practical for medical device manufacturers to focus on new product design.

The IVUS products that utilise this exemption have several unique advantages over other IVUS products which are:

- Co-registration is possible - This means the IVUS images can be mapped to the angiogram (X-ray image) to facilitate image interpretation and easy length measurements without a mechanical "pullback device"
- These are digital catheters as opposed to all other rotational intravascular imaging tools. This means that they have no moving parts, no need for a motor drive to be attached and therefore can be operated with a simplified plug-and-play ease of use. Other types of IVUS device require complex flushing protocols and 2-person bagging of a motor drive/pullback device prior to use, extending the set up time. The digital IVUS catheters can simply be plugged in after a standard flush for immediate imaging so that more patients can be treated per day.

- Some of the IVUS catheters operate at 20 MHz which enables a greater depth of penetration than higher frequency devices. This means they may have advantages in identifying the vessel wall and plaque burden[5], important in selecting the start and end of the lesion when planning for stent implantation and optimizing stent size, diameter and length. The ADAPT DES study[6] demonstrated the value of IVUS imaging for reduced Major Adverse Cardiovascular Events (MACE) rates and Takahashi illustrated the relationship between plaque burden and restenosis. The Mintz review paper is provided for additional reference[7].
  - The OPINION study showed the IVUS requires less (or no) contrast agents than optical coherence tomography (OCT), a light based alternative imaging technique. Ability to use less contrast agents may be important for renal insufficient patients, to avoid acute kidney injury or need for dialysis[8].
  - Several other studies have demonstrated the advantages of digital IVUS catheters[9].
    - The PV IVUS catheters provide multiple advantages:
      - Vessel sizing- helps the physician identify the vessel wall,

[5] Habara. Circ Cardiovasc Interv. 2012; 5:00-00

[6] B. Witzenbichler, et. al., "Relationship Between Intravascular Ultrasound Guidance and Clinical Outcomes After Drug-Eluting Stents" Downloaded from https://www.ahajournals.org/doi/full/10.1161/CIRCULATIONAHA.113.003942

[7] IVUS-Guided Versus OCT-Guided Coronary Stent Implantation. A Critical Appraisal, Mintz et al, Downloaded from http://imaging.onlinejacc.org/content/jimg/10/12/1487.full.pdf

[8] OPINION study presented by Takashi and Akasaka at EuroPCR 2015 Takahashi, M., et al. (2015). "Impact of the distance from the stent edge to the residual plaque on edge restenosis following everolimus-eluting stent implantation." PLoS One 10(3): e0121079

[9] A summary is available at https://www.vasculardiseasemanagement.com/content/limitations-angiography-guiding-peripheral-vascular-interventions

diameter and area of vessel, all of which guides the physician in choosing the optimal treatment. Determining these accurately is important as too large or too small stents can cause further health problems.

- Morphology and geometry- these help the physician to identify plaque, clots, dissections, etc. in order to treat optimally.

- In the peripheral venous space, the VIDIO study (Venography versus intravascular ultrasound for diagnosing and treating iliofemoral vein obstruction) showed that venography identified stenotic lesions in 51 of 100 patients, whereas IVUS identified lesions in 81 of 100 patients. Compared with IVUS, the diameter reduction was on average 11% less for venography ($p<0.001$). The intraclass correlation coefficient was 0.505 for vein diameter stenosis calculated with the two methods. IVUS identified significant lesions not detected with three-view venography in 26.3% of patients.

- If this exemption is not renewed, production stop of the current models will have negative consequences for EU patients'.

☐ Possible social impacts external to the EU

☐ Other : _____

2) Provide sufficient evidence (third-party verified) to support your statement:

9. Other relevant information

Please provide additional relevant information to further establish the necessity of your request:

- Texas Instruments, "Flip Chip Ball Grid Array Package Reference Guide." Some illustrations and materials were obtained from this document with the approval of Texas Instruments[10].
- J. Libres, "Investigation of Bump Crack and Deformation on Pb-Free Flip Chip Packages", in Proc. IEEE Electronic Components and Technol. Conf. (ECTC), Las Vegas, NV, Jun 01-04, 2010, pp. 1536–1540.
- J. Libres, "Challenges in the Assembly ofLarge Die, High Bump Density Pb-Free Flip Chip Packages", in Proc. IEEE/CPMT International Electronic Manufacturing Technology Symposium, San Jose, CA, Oct 03-05, 2007, pp. 346–350.
- Nan Jiang, Liang Zhang, Zhi-Quan Liu, Lei Sun, Wei-Min Long, Peng He, Ming-Yue Xiong & Meng Zhao (2019) Reliability issues of lead-free solder joints in electronic devices, Science and Technology of Advanced Materials, 20:1, 876-901

C.Henderson, " Lead Free Solders—General Issues", Semitracks Monthly Newsletter, Issue 97

10. Information that should be regarded as proprietary

[10] Texas Instruments Flip Chip Ball Grid Array Package Reference Guide, http://www.ti.com/lit/ug/spru811a/spru811a.pdf

Please state clearly whether any of the above information should be regarded to as proprietary information. If so, please provide verifiable justification:

none